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RESEARCH ARTICLE OPEN ACCESS

Automatic Test Pattern Generation for Digital Circuits

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ABSTRACT

Digital circuits complexity and density are increasing and at the same time it should have more quality and reliability. It leads with high test costs and makes the validation more complex. The main aim is to develop a complete behavioral fault simulation and automatic test pattern generation (ATPG) system for digital circuits modeled in verilog and VHDL. An integrated Automatic Test Generation (ATG) and Automatic Test Executing/Equipment (ATE) system for complex boards is developed here. An approach to use memristors (resistors with memory) in programmable analog circuits. The Main idea consists in a circuit design in which low voltages are applied to memristors during their operation as analog circuit elements and high voltages are used to program the memristor's states. This way, as it was demonstrated in recent experiments, the state of memristors does not essentially change during analog mode operation. As an example of our approach, we have built several programmable analog circuits demonstrating memristor -based programming of threshold, gain and frequency. In these circuits the role of memristor is played by a memristor emulator developed by us. A multiplexer is developed to generate a class of minimum transition sequences. The entire hardware is realized as digital logical circuits and the test results are simulated in Model sim software. The results of this research show that behavioral fault simulation will remain as a highly attractive alternative for the future generation of VLSI and system-on-chips (SoC).

Keywords – Automatic test equipment, Comparable circuit for parallel testing, Memristor, Schmitt trigger

I. INTRODUCTION

The design complexities and density of digital circuits in recent years is a growing which leads to the exponential rise in the test generation complexity and an increasing need for high quality test vectors. Circuit boards test is crucial to digital system design, and high test costs make the validation of VLSI circuits more and more critical which can be overcome by ATE System. Two main categories of ATE machines are available nowadays on the market: high-end ATE and low-cost ATE. For example Verigy , Advantest are high-end ATE and others trademarks participate in a competition in the arena of low-cost ATE Inovys , Nextest High-end ATEs are characterized by high grade of automation on the other hand they are very expensive and require an accurate setup and skilled people so ASIC manufacturers also needs some other testing solution, which can be executed in house during preliminary chip evaluation phase.

In this paper we propose we suggest an approach to use memristors (resistors with memory) in programmable analog circuits. Our idea consists in a circuit design in which low voltages are applied to memristors during their operation as analog circuit elements and high voltages are used to program the memristor's states. This way, as it was demonstrated in recent experiments, the state of memristors does not essentially change during analog mode operation. As an example of our approach, we have built several programmable analog circuits demonstrating memristor -based programming of threshold, gain and frequency. In these circuits the role of memristor is played by a memristor emulator developed by us.

There are two types of ATG Random ATG and Deterministic ATG. Random ATG is less complex than deterministic ATG. Random ATG may be able to quickly generate tests initially, but it would be very inefficient to achieve higher fault coverage. Deterministic ATG can be applied to both combinational circuits and sequential circuits. In practice sequential ATG is in orders of magnitude more complex than combinational ATG. D-algorithm ,PODEM and FAN algorithm is commonly used path sensitizer. Most ATG using stuck-at at fault model can't deduce tests for complex circuit boards with LSI/VLSI.

Unlike most other deterministic ATG using the stuck-at fault model, Behavioral based automatic test generation(BBATG) technique is proposed which use the device behavior fault model which can completely describe functions and timing relations for a combination or sequence device, and then needn't decompose devices to gate-level descriptions. At the same time, we use the structural model to describe circuit board as an interconnection of devices.

The paper is organized as follows: Section II discusses the need for memristor applicayion. Section III presents the Schmitt trigger application. The comparable circuit with parallel testing using DRAM is presented in section IV The simulation results with different parameter evaluation are presented in section V. Finally, conclusions and future work are given in section VI.

II. MEMRISTOR APPLICATION

An array of 17 purpose-built oxygen-depleted titanium dioxide memristors built at HP Labs, imaged by an atomic force microscope. The wires are about 50 nm, or 150 atoms, wide. Electric current through the memristors shifts the oxygen vacancies, causing a gradual and persistent change in electrical resistance Memristor (pronounced /□ m□mr□st□ r/; a portmanteau of "memory resistor") is a name of passive two-terminal circuit elements in which the resistance is a function of the history of the current through and voltage across the device and is expressable in terms of a functional relationship between charge and magnetic flux linkage. Memristor theory was formulated and named by Leon Chua in a 1971 paper. On April 30, 2008, a team at HP Labs announced the development of a switching memristor based on a thin film of titanium dioxide[citation needed]. It has a regime of operation with an approximately linear charge-resistance relationship as long as the time-integral of the current stays within certain bounds.[4][5][6][7] These devices are being developed for application in nanoelectronic memories, computer logic, and neuromorphic computer architectures.

Memristor symbol

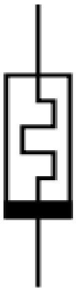

Fig.1: Memristor symbol

A memristor is a passive two-terminal electronic component for which the resistance (dV/dI) depends in some way on the amount of charge that has flowed through the circuit. When current flows in one direction through the device, the resistance increases; and when current flows in the opposite direction, the resistance decreases, although it must remain positive. When the current is stopped, the component retains the last resistance that it had, and when the flow of charge starts again, the resistance of the circuit will be what it was when it was last active.

Applications of Memristor

- Memristor-based programmable Threshold comparator
- Memristor-based switching threshold Schmitt trigger
- Memristor-based Programmable gain amplifier
- Memristor-based Programmable frequency oscillator

PROGRAMMABLE ANALOG CIRCUITS

Memristors in Programmable Analog Circuits Our main idea of using memristors in analog circuits is based on the following observation of the experimental results: the rate of memristance change depends essentially on the magnitude of applied voltage At voltages below a certain threshold, the change of memristance is extremely slow, whereas at voltages above the threshold, , it is fast. Therefore, we suggest to use memristors in analog circuits in such away that in the analog mode of operation (when the memristor performs a useful function as an analog circuit element) only voltages of small magnitude (below the threshold) are applied to the device, while higher-amplitude voltages (above the threshold) are used only for programming.

The programming voltages can be applied in the form of pulses. Each pulse changes the resistance of memristor by a discrete amount. In this way, programmable memristors operate basically as digital potentiometers. However, there are several potential advantages of memristor-based digital potentiometers over the traditional ones. In particular, the size of a memristor can be very small, down to 30 nm , allowing for higher density chips/smaller electronic components.

The memristor is essentially a two-terminal variable resistor, with resistance dependent upon the amount of charge q that has passed between the terminals.

$$V = I \cdot M(q)$$

To relate the memristor to the resistor, capacitor, and inductor, it is helpful to isolate the term M(q), which characterizes the device, and write it as a differential equation. where Q is defined by $I = dQ/dt$, and Φ_m is defined by $V = d\Phi_m/dt$. Note that the above table covers all meaningful ratios of I, Q, Φ_m, and V. No device can relate I to Q, or Φ_m to V, because I is the derivative of Q and Φ_m is the integral of V.

The variable Φ_m ("magnetic flux linkage") is generalized from the circuit characteristic of an inductor. It does not represent a magnetic field here, and its physical meaning is discussed below. The symbol Φ_m may simply be regarded as the integral of voltage over time.

Thus, the memristor is formally defined as a two-terminal element in which the flux linkage (or integral of voltage) Φ_m between the terminals is a function of the amount of electric charge Q that has passed through the device. Each memristor is characterized by its memristance function describing the charge-dependent rate of change of flux with charge.

$$M(q) = \frac{\mathrm{d}\Phi_m}{\mathrm{d}q}$$

Substituting that the flux is simply the time integral of the voltage, and charge is the time integral of current, we may write the more convenient form

$$M(q(t)) = \frac{\mathrm{d}\Phi_m/\mathrm{d}t}{\mathrm{d}q/\mathrm{d}t} = \frac{V(t)}{I(t)}$$

It can be inferred from this that memristance is simply charge-dependent resistance. If M(q(t)) is a constant, then we obtain Ohm's Law R(t) = V(t)/ I(t). If M(q(t)) is nontrivial, however, the equation is not equivalent because q(t) and M(q(t)) will vary with time. Solving for voltage as a function of time we obtain

$$V(t) = M(q(t))I(t)$$

This equation reveals that memristance defines a linear relationship between current and voltage, as long as M does not vary with charge. Of course, nonzero current implies time varying charge. Alternating current, however, may reveal the linear dependence in circuit operation by inducing a measurable voltage without net charge movement—as long as the maximum change in q does not cause much change in M.

Furthermore, the memristor is static if no current is applied. If I(t) = 0, we find V(t) = 0 and M(t) is constant. This is the essence of the memory effect.

The power consumption characteristic recalls that of a resistor, I^2R.

$$P(t) = I(t)V(t) = I^2(t)M(q(t))$$

As long as M(q(t)) varies little, such as under alternating current, the memristor will appear as a constant resistor. If M(q(t)) increases rapidly, however, current and power consumption will quickly stop.

[edit] Derivation of "flux linkage" in a passive device

In an inductor, magnetic flux Φ_m relates to Faraday's law of induction, which states that the energy to push charges around a loop (electromotive force, in units of Volts) equals the negative derivative of the flux through the loop:

$$\mathcal{E} = \frac{-\mathrm{d}\Phi_\mathrm{m}}{\mathrm{d}t}$$

This notion may be extended by analogy to a single device. Working against an accelerating force (which may be EMF, or any applied voltage), a resistor produces a decelerating force, and an associated "flux linkage" varying with opposite sign. For example, a high-valued resistor will quickly produce flux linkage. The term "flux linkage" is generalized from the equation for inductors, where it represents a physical magnetic flux: If 1 Volt is applied across an inductor for 1 second, then there is 1 V·s of flux linkage in the inductor, which represents energy stored in a magnetic field that may later be obtained from it. The same voltage over the same time across a resistor results in the same flux linkage (as defined here, in units of V-s), but the energy is dissipated, rather than stored in a magnetic field — there is no physical magnetic field involved as a link to anything. Voltage for passive devices is evaluated in terms of energy lost by a unit of charge, so generalizing the above equation simply requires reversing the sense of EMF.

$$V = \frac{\mathrm{d}\Phi_\mathrm{m}}{\mathrm{d}t}$$

$$\Phi_\mathrm{m} = \int V\,\mathrm{d}t$$

Observing that Φ_m is simply equal to the integral over time of the potential drop between two points, we find that it may readily be calculated, for example by an operational amplifier configured as an integrator.

Two unintuitive concepts are at play:

- Magnetic flux is defined here as generated by a resistance in opposition to an applied field or electromotive force. In the absence of resistance, flux due to constant EMF, and the magnetic field within the circuit, would increase indefinitely. The opposing flux induced in a resistor must also increase indefinitely so the sum with applied EMF remains finite.
- Any appropriate response to applied voltage may be called "magnetic flux," as the term is used here.

The upshot is that a passive element may relate some variable to flux without storing a magnetic field. Indeed, a memristor always appears instantaneously as a resistor. As shown above, assuming non-negative resistance, at any instant it is dissipating power from an applied EMF and thus has no outlet to dissipate a stored field into the circuit. This contrasts with an inductor, for which a magnetic field stores all energy originating in the potential across its terminals, later releasing it as an electromotive force within the circuit.

Physical restrictions on M(q)

M(q) is physically restricted to be positive for all values of q (assuming the device is passive and does not become superconductive at some q). A negative value would mean that it would perpetually supply energy when operated with alternating current.An applied constant voltage potential results in uniformly increasing Φ_m. It is not realistic for the function M(q) to contain an infinite amount of information over this infinite range. Three alternatives avoid this physical impossibility:

- M(q) approaches zero, such that $\Phi_m = \int M(q)dq = \int M(q(t))I(t)\,dt$ remains bounded but continues changing at an ever-decreasing rate. Eventually, this would encounter some kind of quantization and non-ideal behavior.
- M(q) is periodic, so that $M(q) = M(q - \Delta q)$ for all q and some Δq, e.g. $\sin^2(q/Q)$.
- The device enters hysteresis once a certain amount of charge has passed through, or otherwise ceases to act as a memristor.

III. MEMRISTOR WITH SCHMITT TRIGGER

DESIGN

- Semiconductor based memristance can be designed by the semiconductor industry , like how they designing the diodes, transistors , inductors , capacitors etc
- In our project we are experimentally showing the working of the MEMRISTOR and their few useful applications
- We designed a concept called Memory which is capable of storing the calculated resistance values

STEP 1: CALCULATING RESISTANCE VALUES AND STORING IN THE MEMORY
Initial resistance value to be 100 ohms
Maximum resistance value to be 10 kilo ohms
In between a sweep of resistance with a increment step size of 38.66 is added up
That is, Default 100ohms,
If one step increase in input voltage , now resistance value will be 100+38.66 = 138.66 ohms
If input voltage increased 2 step ,now resistance value will be 100+(38.66 x 2) = 177.32 ohms
Like this the resistor values are being calculated and stored in a memory designed using a “n” Bit Multiplexer

STEP 2: DESIGN OF SCHMITT TRIGGER WITH MEMRISTOR
SCHMITT TRIGGER CONCEPT
Schmitt trigger is a pulse shaping circuit , Used to convert input sine wave to square wave.
GENERAL EXPRESSION USED FOR SCHMITT TRIGGER

V upper threshold = (Rmemristor / Rstandard) X Vsat

V lower threshold = - (Rmemristor / Rstandard) X Vsat

Where
Rstandard = any standard resistor value
Rmemristor = Replaced with MEMRISTOR
Vsat = input constant voltage

So depends upon the Change in MEMRISTOR value, the pulse shaping of the memristor getting changed.

MEMRISTOR-BASED NEURAL LOGIC BLOCKS FOR NONLINEARLY SEPARABLE FUNCTIONS EXISTING BLOCK

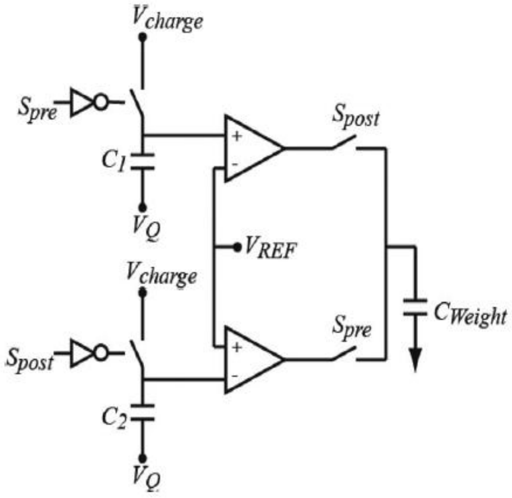

Fig.2: Existing block

RE-MODELLED LOGIC DIAGRAM

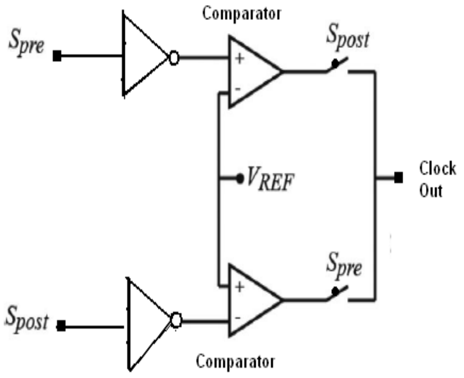

Fig.3 : Remodelled logic diagram

- Neural blocks are nothing but the standard design logic blocks which will be connected based on certain algorithms
- The purpose of connecting this blocks is to perform positive and negative combinations.
- Simple neural blocks are used to create on chip networks to perform the required tast in high speed.
- System – on – chip is the base for creating such blocks.

BLOCK DIAGRAM OF ATPG

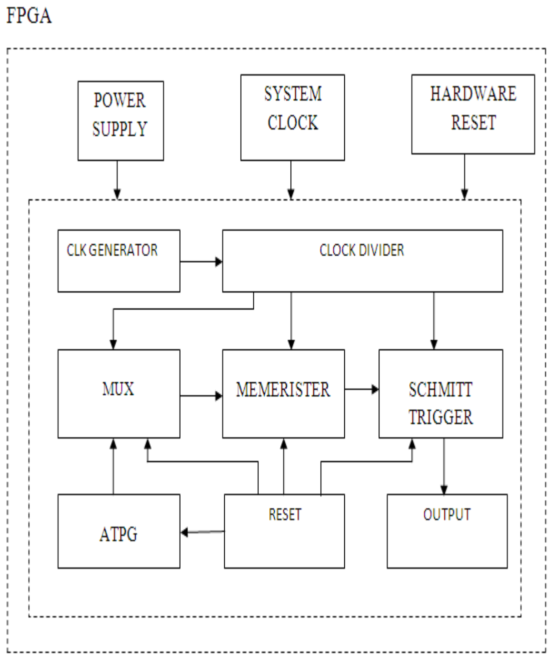

Fig .4 : Block diagram

MULTIPLEXER MODULE

In this module, the multiplexer is designed and analyzed. The multiplexer is used in this module is to first select the different test patterns to test the device. After testing, the multiplexer is used to select the memristor data input.

MEMRISTOR MODULE

In second module we design the memristor as the one of the application. Before using the device in particular application we conduct the test procedure and after that used in the application as memristor.

SCHMITT TRIGGER MODULE

In this module we design another one of the application as Schmitt trigger. The inputs to the Schmitt trigger is taken from the memory and performs the operation of Schmitt trigger and analyze the output.

IV. COMPARABLE CIRCUIT WITH PARALLEL TESTING

This is the another circuit for testing using DRAM. The simulation is done using Model sim and the coding is written in VHDL.

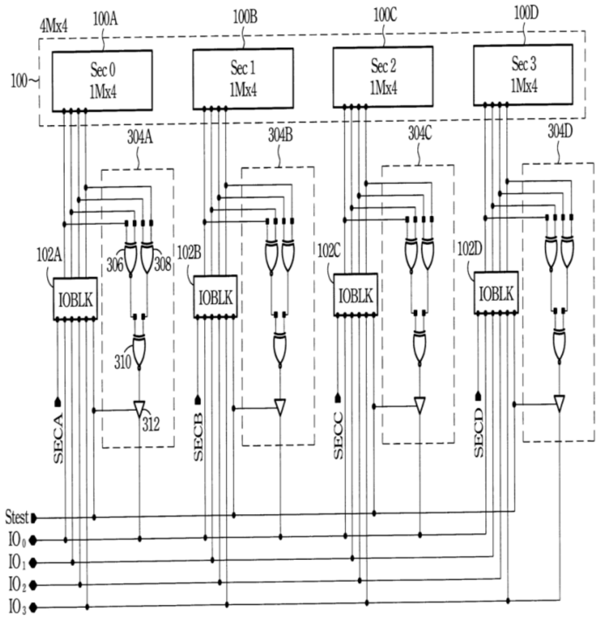

Fig. 5: Example DUT for test

V. SIMULATION RESULTS

The proposed system has been successfully used to test tens of prototypes of two Systems on Chip (SoC) developed to realize control systems based on Micro Electro Mechanical (MEM) sensors. A detection test is to find if a circuit has a behavior fault. A diagnostic test is to locate the behavior fault inside the circuit.

MODULE 1 OUTPUT

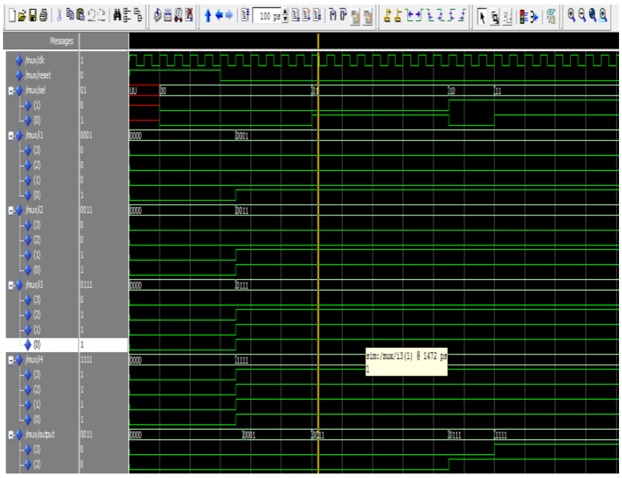

Fig .6 : Multiplexer output

The module 1 is the multiplexer output which is already explained in the block diagram. In this module, the multiplexer is designed and analyzed. The multiplexer is used in this module is to first select the different test patterns to test the device. After testing, the multiplexer is used to select the memristor data input.

MODULE 2 OUTPUT

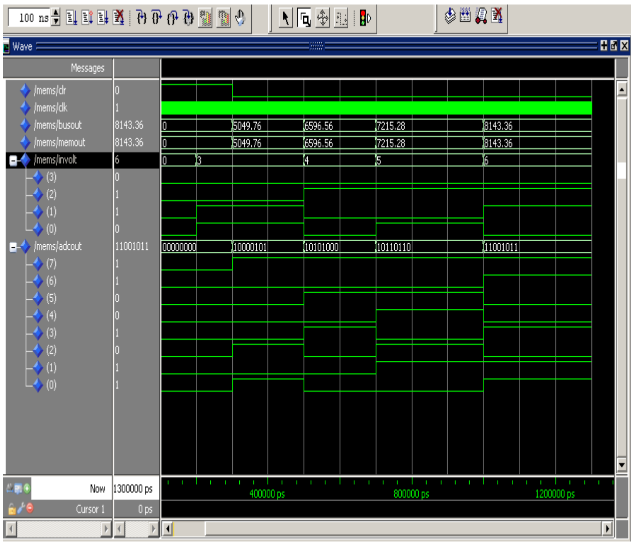

Fig.7: Memristor output

The second module is memristor module. In second module, the design of memristor is the first application. Before using the device in particular application we conduct the test procedure and after that used in the application as memristor.

MODULE 3 OUTPUT

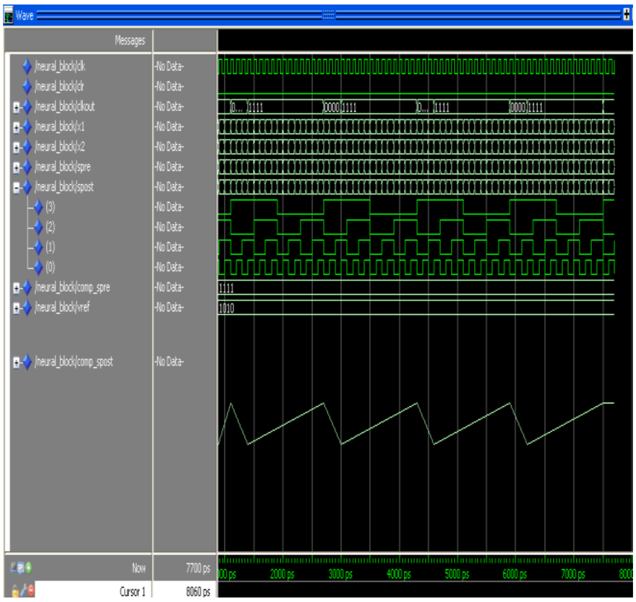

Fig.8: Schmitt trigger

This is the Schmitt trigger output. In this module we design another one of the application as Schmitt trigger. The inputs to the Schmitt trigger is taken from the memory and performs the operation of Schmitt trigger and analyze the output.

VI. DISCUSSION AND CONCLUSION

In this paper, automatic test equipment to validate the each and every digital parts of VLSI chip. A simple test patterns are generated based on the behavioral functionalities of any DUT is processed and loaded to the memory by FSM. Based on that DUT stimulus is generated, tested and samples should be collected. Testing of both synchronous and asynchronous circuits is tested. An interesting reduction in the overall test duration can be achieved by using an external flash memory to store all test patterns. The results of this research show that behavioral fault simulation will remain as a highly attractive alternative for the future generation of VLSI and system-on-chips (SoC). Areas of future research include the refinement of existing faults and defining new behavioral faults to reduce the gap between the behavioral fault models and gate level failures and the development of a better test pattern generator for each target faults. Another valuable enhancement would be to run fault simulation in parallel, by embedding multiple faulty models into one test bench to simulate many faults concurrently. This would speed up the behavioral fault simulation than the gate based synthesis.

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REFERENCES

[1] Huxun Chen, DeQing Chen, Jinlin Ye, Weizhou Cao, Lei Gao "An Integrated Automatic Test Generation and Executing System" IEEE Conference Sept 2011.

[2] Luca Mostardini, Luca Bacciarelli, Luca Fanucci, Lorenzo Bertini, Marco Tonarelli "FPGA-based Low-cost Automatic Test Equipment for Digital Integrated Circuits" IEEE International Workshop Sept 2009.

[3] Mohmed Elbably" An Automatic testing of PLDs"Nineteenth National Radio Science Conference ,March 19-23,2002

[4] C. Giaconia, A. Di Stefano, G. Capponi, "Reconfigurable digital instrumentation based on FPGA System-on-Chip for Real-Time Applications," 2003. Proceedings. The 3rd IEEE International Workshop, 30 June-2 July 2003, pp. 120 – 122.

[5] Ranin Roosta, VLSI Test Automation: Fault Modeling, Ph.D Dissertation, EE623, Department of Electrical and Computer

Engineering, California State University, Northridge.

[6] IEEE Std 1149.1-2001, Annex B: “Boundary-scan description language”

[7] http://www.verigy.com/ (Verigy website)

[8] http://www.advantest.com/ (Advantest website)

[9] W. Quddus, A. Jas, and N.Touba, “Contiguration Self-Test In FPGA-Based Reconfigurable Systems,”Master Thesis, Dept. of ECE university of Texas at Austin, May 1999.

[10] http://www.inovys.com/ (Inovys website)

[11] http://www.nextest.com/ (Nextest website)

[12] S. Hauch, “The roles on FPGA’s in reprogrammable systems,” in Proceedings of The IEEE, vol. 86, no. 4, April 1998.

[13] S. Konala, P. Chen, and M. Abramovici, “Built-In-Self-Test of Logic Blocks in FPGAs,” Proc. IEEE VLSI Test Symposium, 1996, pp. 387-392.

[14] C. Stroud, E. Lee, S. Yonala, and M. Abramovici, “Using ILA Testing for BIST in FPGAs,” Proc. Of International Test Conference IEEE, 1996, pp. 68-75.

[15] E.M. Saad, I.E. Talkhan, I.M. Sayed, “A proposed ATE for digital systems Radio Science Conference,” 1996. NRSC '96., Thirteenth National, 19-21 March, 1996, pp. 209 – 220.